Master PCIe Gen5/6 Measurement Techniques and Challenges

MASTER YOUR NEXT DESIGN

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2021.12

Solutions Engineer / Keysight Technologies

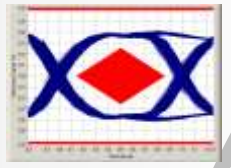
KEYSIGHT TECHNOLOGIES

Agenda

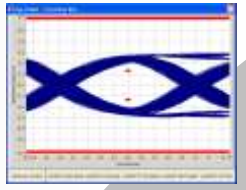
- **PCIe 5.0 CEM Tx/Rx Test Consideration**
  - Gen5 CEM Fixture timeline
  - Phy Test Specification update
  - 100MHz System Clock jitter test update
- **PCIe 6.0 64GT/s Test Consideration Pathfinding**
  - PAM4, SSC, SNDR, Top EH/EW
- **M8040A BERT solution for PCIe 5.0/6.0 LinkEQ Testing**
  - HS digital applications coverage
  - Redriver and EQ for long channel system board
  - Firmware evolution & HW performance
  - Fast, Accurate Rx Compliance SW
- **Summary**

PCI Express Technology Roadmap

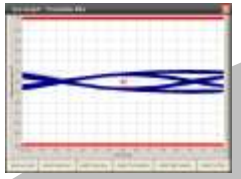
- PCIe doubles the data rate every generation with full backwards compatibility every 3 years
- Ubiquitous I/O across the compute continuum: PC, Hand-held, Workstation, Server, Cloud, Enterprise, HPC, Embedded, IoT, Automotive, AI



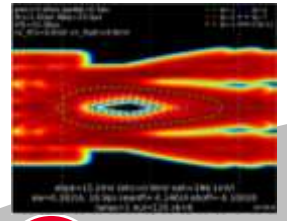
2003
PCIe 1.0 (2.5 GT/s)



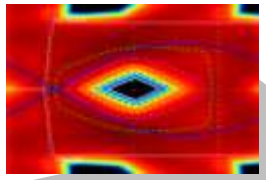
2006
PCIe 2.0 (5 GT/s)



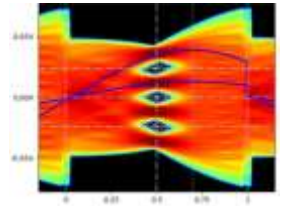
2010
PCIe 3.0 (8 GT/s)



2017
PCIe 4.0 (16 GT/s)



2019
PCIe 5.0 (32 GT/s)



2022 **BASE 6.0 v1.0 Oct 2021**
PCIe 6.0 (64 GT/s)

PCI Express 5.0 Specifications and Scope

SELECT THE SPECIFICATIONS FOR YOUR SPECIFIC NEED

Base Specification
- Contains all the system knowledge
- Can directly be applied to Chip Test

PCIe 5.0 BASE
Released 1.0 May 2019

Card Electromechanical (CEM) Spec
- Applies to add-in cards and mother boards
- Mitigates card manufacturer's need to study the base specification
- Increases reproducibility through PCI-SIG supplied test tools CBB and CLB (compliance base and load board)

PCIe_CEM_SPEC_R5_V1.0
Released in June 2021

Phy Test Specification
- Defines compliance tests of CEM spec in detail

Latest
PCIe_5_0_PHY_Test_Spec_Ver0.9
Released Oct. 2021

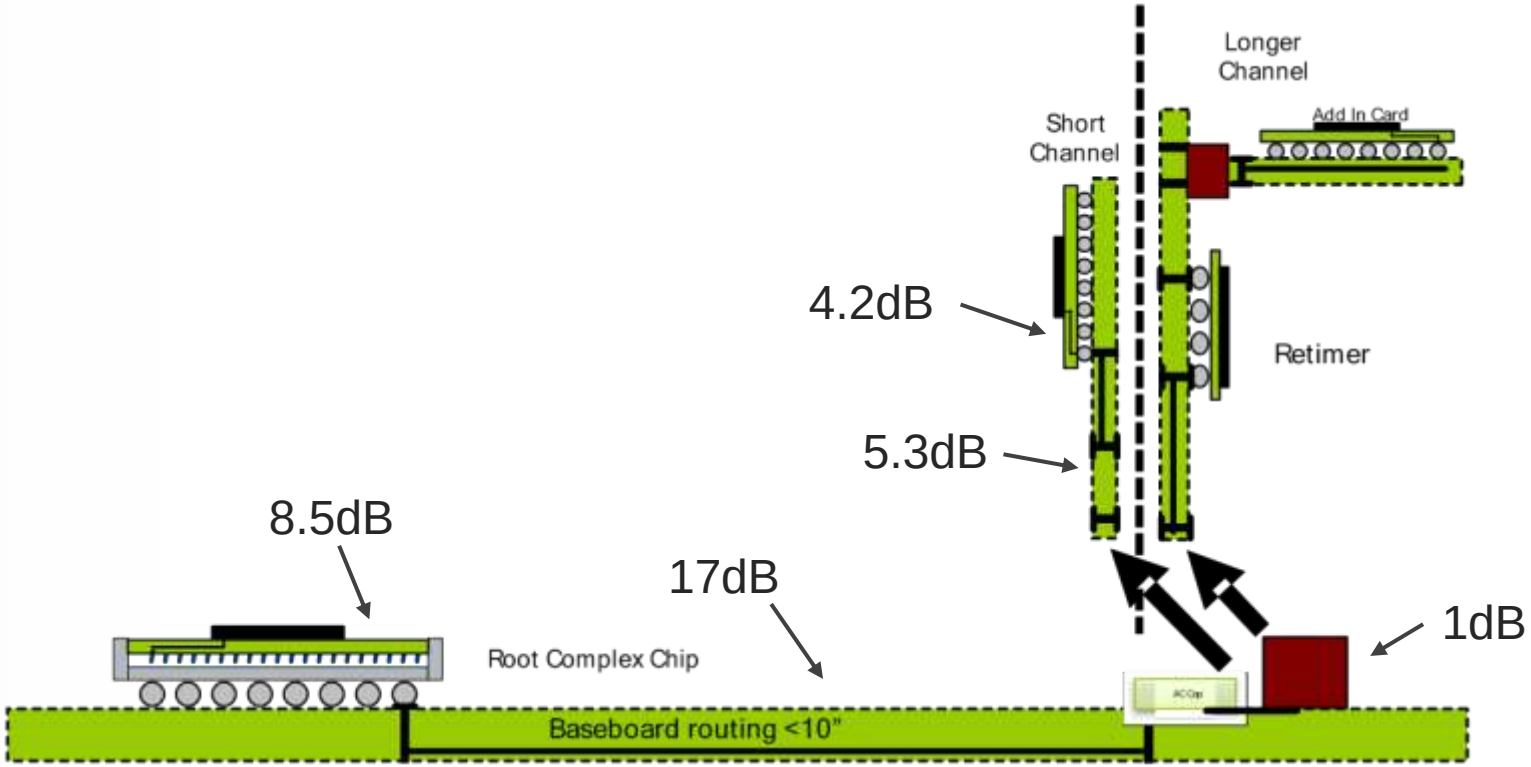
PCIe 5.0 – Goals

DELIVERING THE FASTEST PCIE SPEED YET

- PCIe 5.0 is backwards compatible with prior generations
  - Enhanced SMT connector
  - Same pinout
- Signaling is doubled (vGen4) to 32 GT/s
  - Minimal spec changes – only ones needed to enable speed bump
  - EIEOS changed to maintain frequency
  - Encoding remains 128/130
  - Loss budget: Goal 35-36 dB
  - Equalization: 8 GT->16 GT-> 32 GT/s
  - > 2x Tx jitter reduction
  - ~3x Reference Clock jitter reduction
  - Improved 32 GT/s Reference CTLE equalization, 3 tap DFE
  - BER target is 10e-12

PCI Express 5.0 Channel Topology

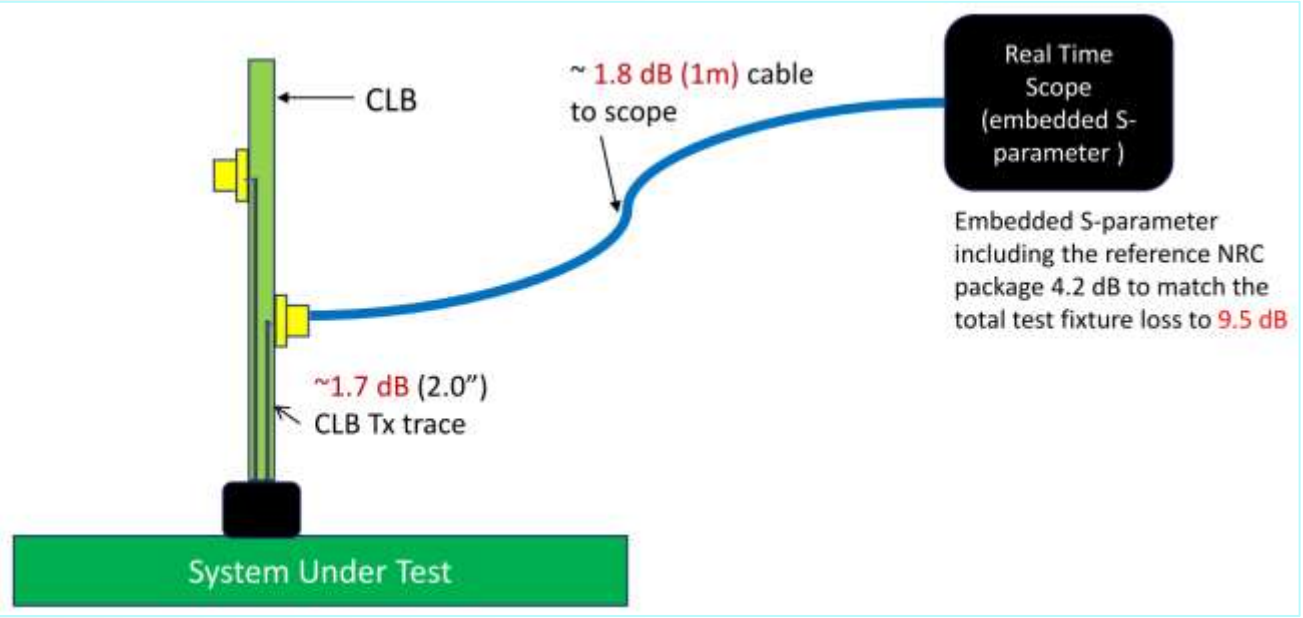
RETIMER REQUIRED WHEN LOSS EXCEEDS -36 DB OR >1 CONNECTOR

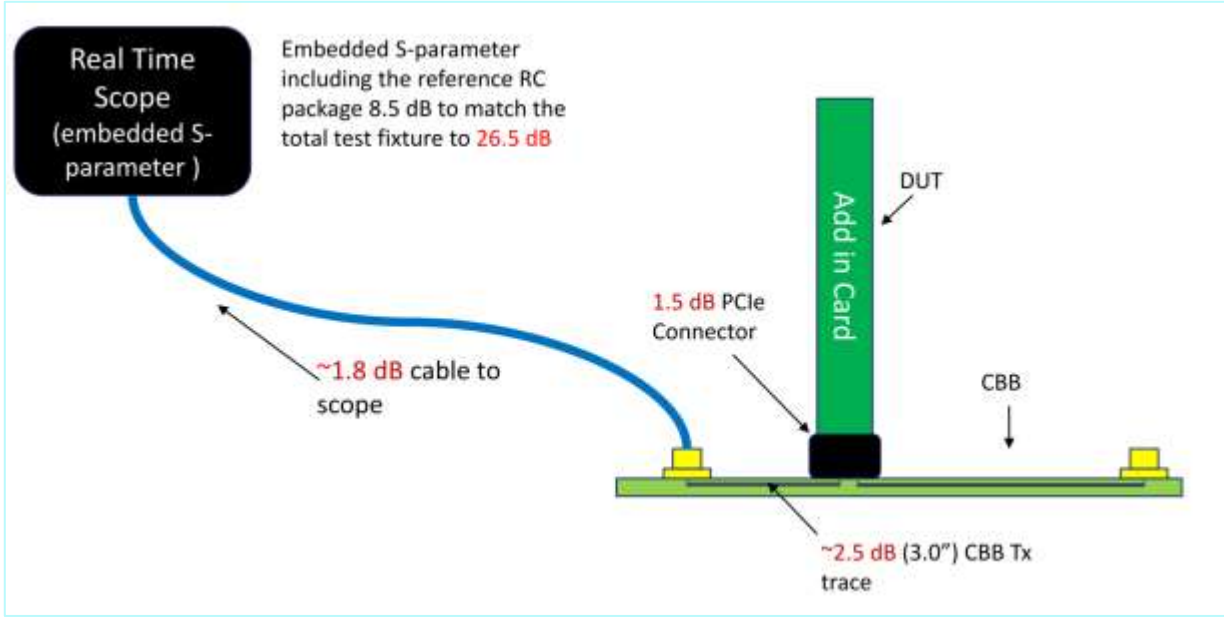


- Estimated allowable loss: ~= -36 dB @ 16 GHz
- Root complex pkg loss allowance ~= -8.5 dB @ 16 GHz
- Add-in Card pkg loss allowance ~= -4.2 dB @ 16 GHz
- Total AIC loss budget estimate = ~9.5 dB @ 16 GHz
- PCIe 5.0 CEM Connector loss budget ~= 1 dB @ 16 GHz

CEM 5.0 System Board/AIC Tx Testing

PCIE PHY TEST SPECIFICATION REV.5.0 V0.9



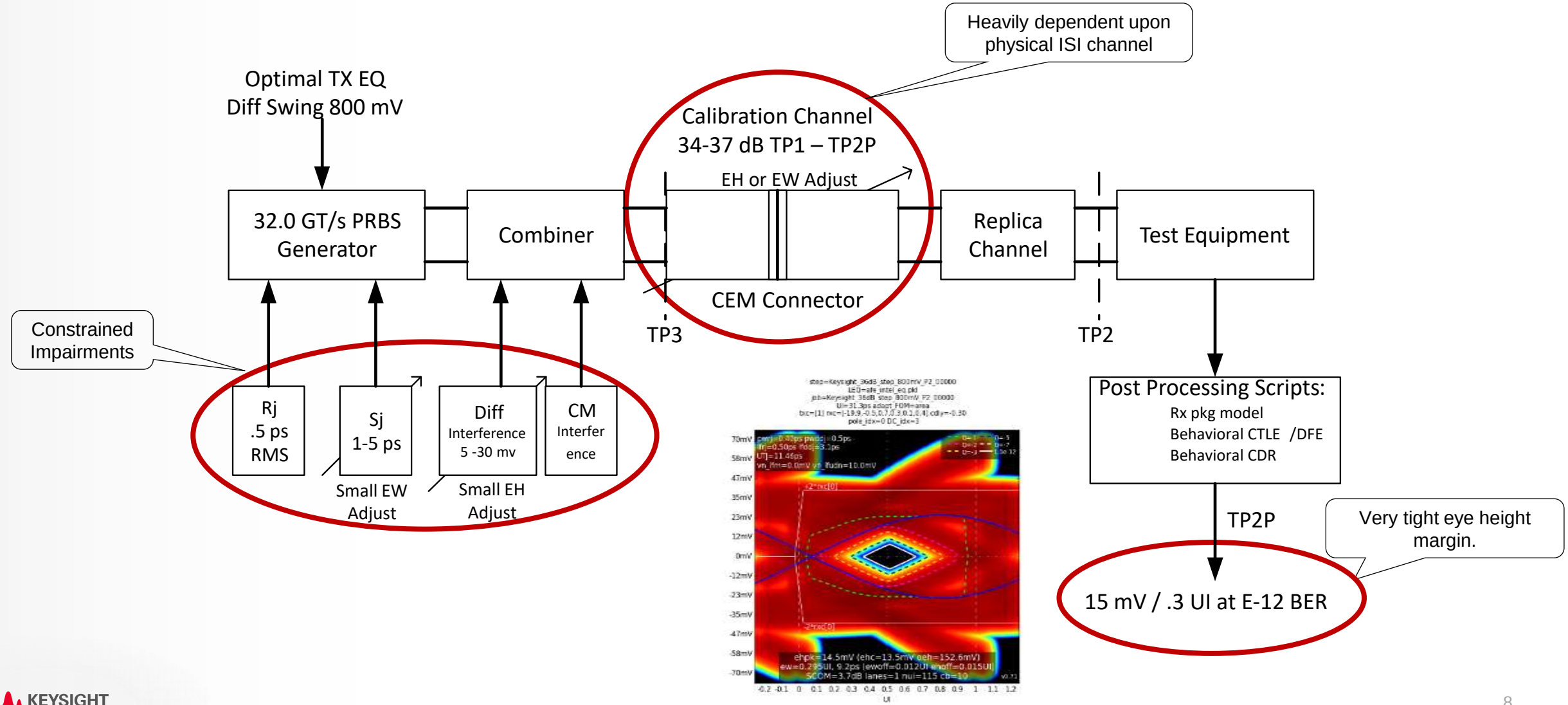


Test with SSC enable or disable

- need to be tested **with SSC enable**
- 2.1.6 AIC Tx Compliance test 32GT/s
- 2.3 AIC Base spec. Jitter test 32GT/s
- 2.4.4 AIC Tx Preset test
- 2.5.4 & 2.6.4 AIC Tx LinkEQ

PCIe 5.0 32 GT/s RX Calibration (BASE)

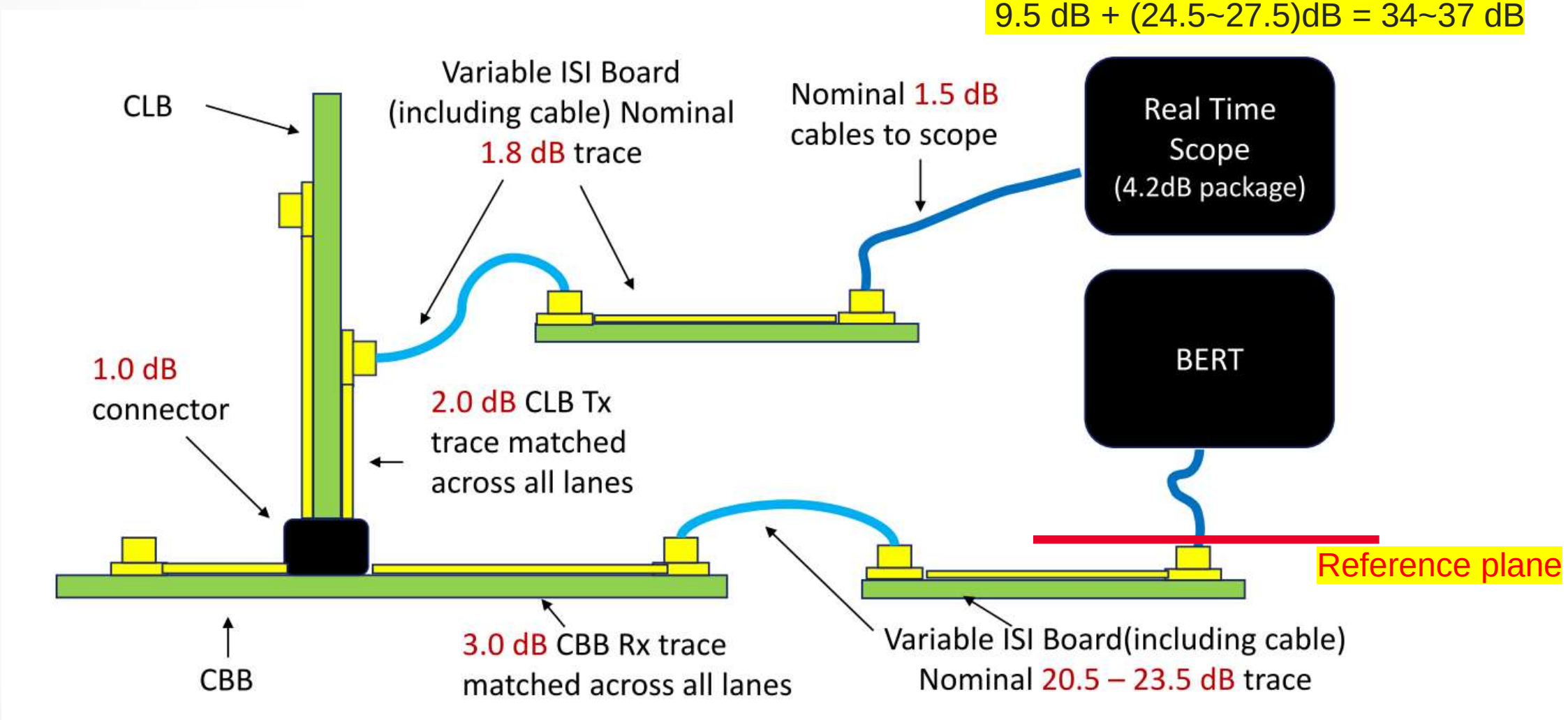
15 MV EYE HEIGHT POST EQ (0.3UI EYE WIDTH) TARGET



CEM 5.0 AIC Rx Stressed Eye Calibration

UPDATED FROM PCI-SIG IN JUNE

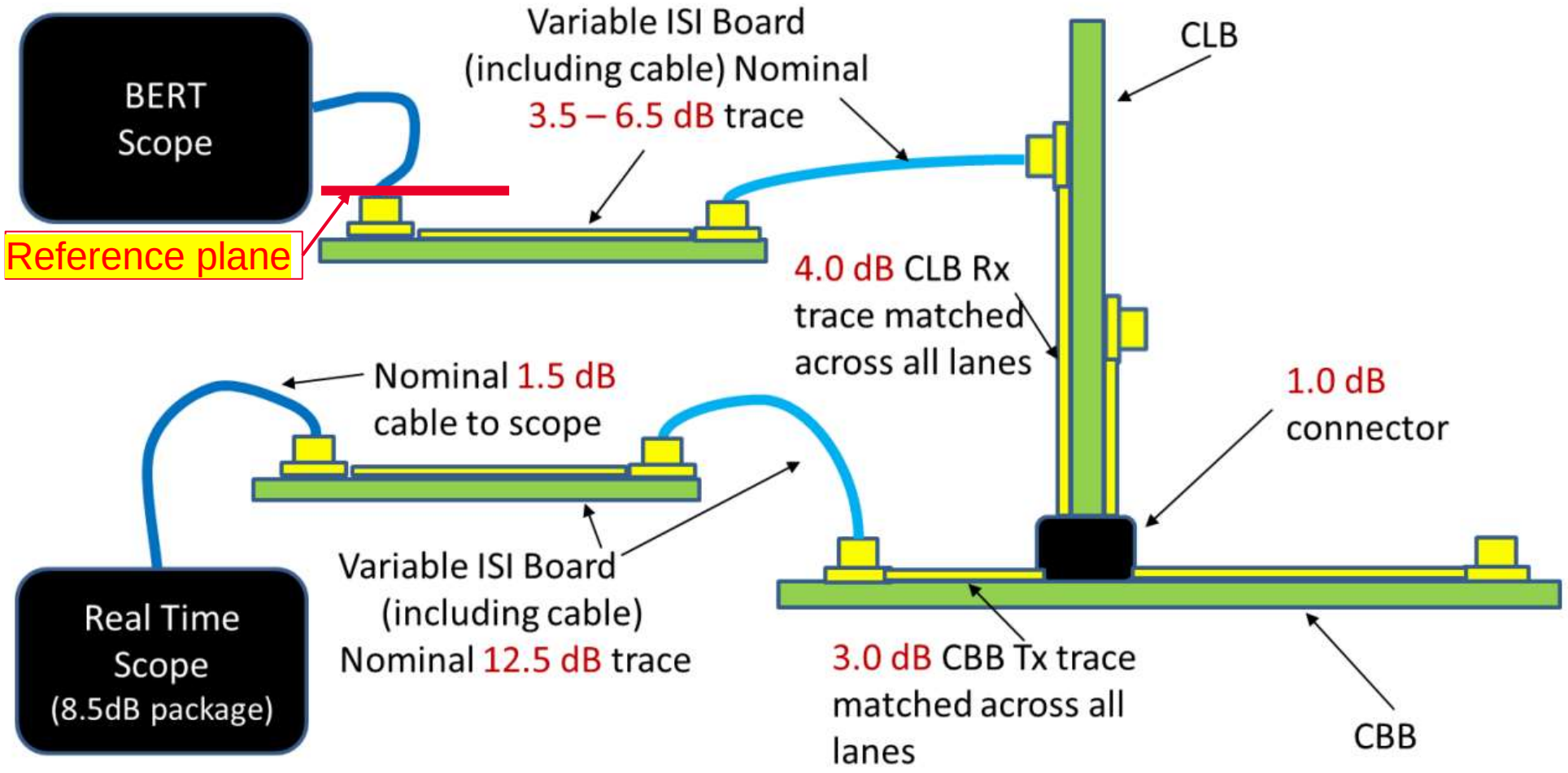
9.5 dB + (24.5~27.5)dB = 34~37 dB



CEM 5.0 System Rx Stressed Eye Calibration

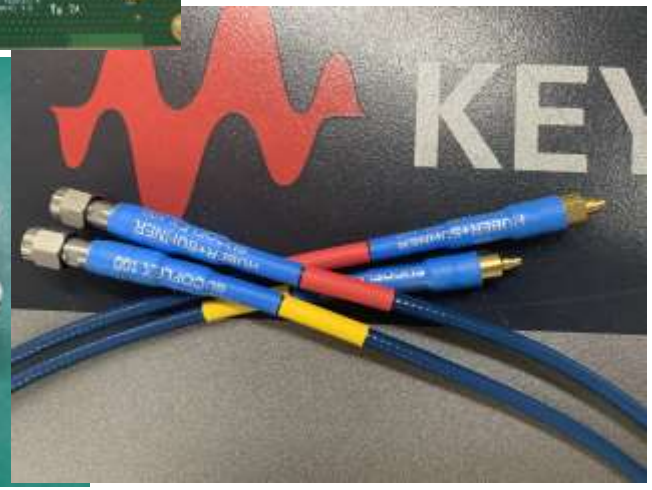
UPDATED FROM PCI-SIG IN JUNE

26.5 dB + (7.5~10.5)dB = 34~37 dB

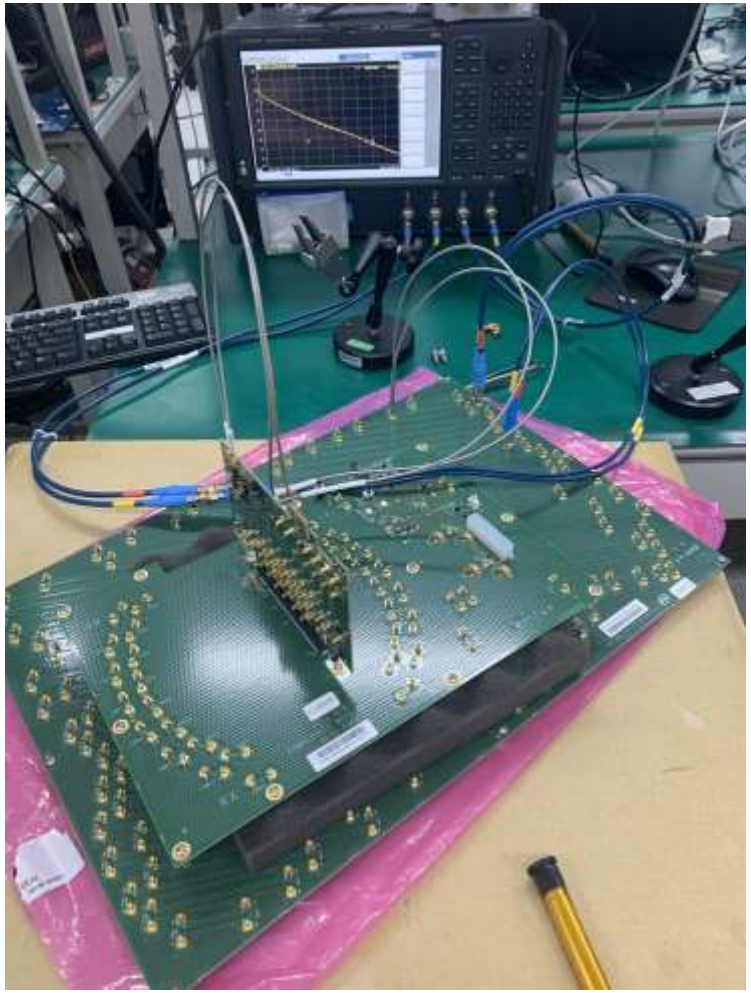


PCIe 5.0 CEM Fixtures

TEST FIXTURES (REVISION 2.0 SHOWN)



- PCIe 5.0 CEM Test Fixtures (rev 3) should Ship from PCI-SIG by Dec. (25 sets), Mar.(75)
- ~13K USD
- MMPX (F) on CBB/CLB/ISI board
- MMPX (m) on cables

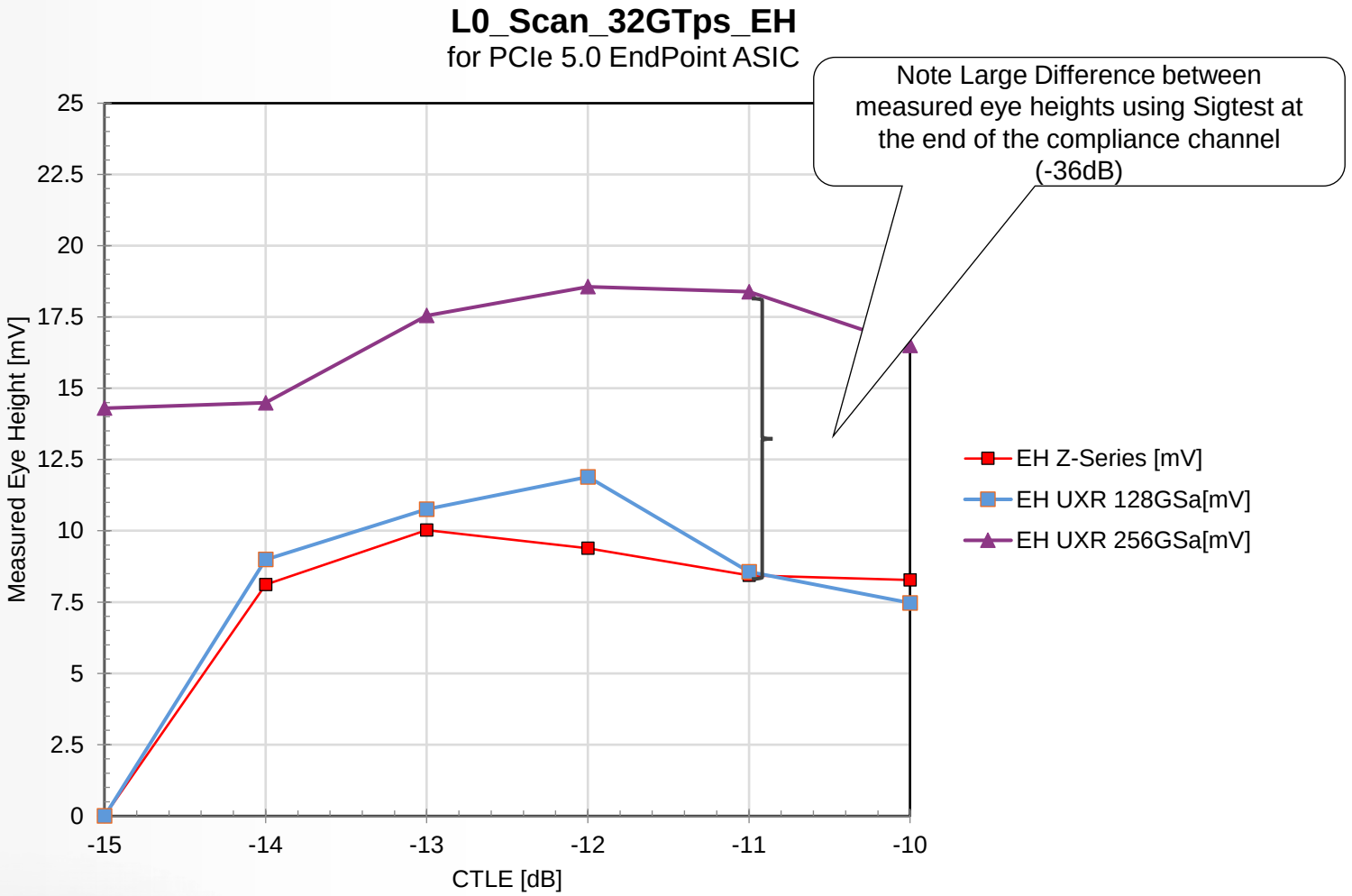


The Industry's Best Signal Integrity

- **10 bits ADC, 256 GSa/s**
- **Lowest noise**
  < 900 µV rms @ 110 GHz
  < 500 µV rms @ 70 GHz
  < 300 µV rms @ 33 GHz
- **Lowest intrinsic jitter**
  20 fs rms
- **Lowest inter-channel jitter**
  10 fs rms
- **Highest ENOB**
  > 5.0 bits @ 110 GHz
  > 5.4 bits @ 70 GHz
  > 5.9 bits @ 33 GHz

UXR vs Z Series: End of Channel Results

NOISE FLOOR MATTERS: EYE HEIGHT* @ 32 GT/S



- Data Rate = 32 Gb/s
- Sigtest Composite Eye Height
  - 2M UI
  - CTLE -10 dB to -15 dB
- M8040A BERT
  - TX preset P5
  - Generator Launch =800 mV
  - DMSI=10 mV
  - CMSI=0 mV
  - RJ=0.5 ps
  - SJ=3.125 ps @ 100 MHz

* Based on waveform analysis using Sigtest

System Board 100MHz Ref. Clock Jitter

PCIE REV.5.0 TEST SPEC. V0.9 DRAFT

2.17 System Board Reference Clock (100 MHz) Jitter Test

The CEM 5.0 specification has removed the requirement to measure the TX signal quality using Dual Port (capturing data and clock), so this test was introduced to ensure the System's 100 MHz reference clock does not violate the CEM 5.0 specification clock jitter limit.

1. Connect the edge mounted SMP's on the CLB to a high-speed oscilloscope or equivalent data capture instrument via phase matched, low loss SMP to 2.92mm cables or SMP to 2.92mm adapters and phase matched, low loss 2.92 to 2.92mm cables. Use appropriate edge mounted SMP's for the CLB card edge used.
2. The system will use SSC enabled or SSC disabled reference clock to be consistent with settings for the system during normal operation.
3. Capture transmitted clock waveform with a high-speed oscilloscope or equivalent data capture instrument with the maximum bandwidth set to 5 GHz. Use sampling rate necessary to minimize aliasing (noise).
4. Confirm that the waveform is the clock waveform at 100 MHz. SSC can be On or Off depending on system configuration (use same SSC configuration as used for TX signal quality test).
5. Capture at least 80,000 clock cycles (80,000 X 10 ns = 0.8 ms).

Note: Real Time Scope noise may be removed during the post-processing steps of this measurement.

8. Measure Rj RMS Jitter, treating all remaining phase noise as random without Rj and Dj separation.
9. If the analysis program indicates that the HF Rj RMS jitter is less than 200 fs, the system clock compliance test passes and is complete.

Sample Rate of 20GSa/s may not be optimal.

Pass requirement is less than 200fs

Using Optimal Sample Rate

SAMPLE RATE SELECTION MADE TO MINIMIZE HF ALIASING AT 5GHZ

Sample Rate

UXR (110GHz BW)				
Sample Rate	Clock Cycles	Max Jitter (ps)	Min Jitter (ps)	Pass/Fail
256 Gsa	160000	0.053119466	0.010370885	Pass

Z-Series (33GHz BW)				
Sample Rate	Clock Cycles	Max Jitter (ps)	Min Jitter (ps)	Pass/Fail
80 Gsa	160000	0.064823283	0.012659228	Pass

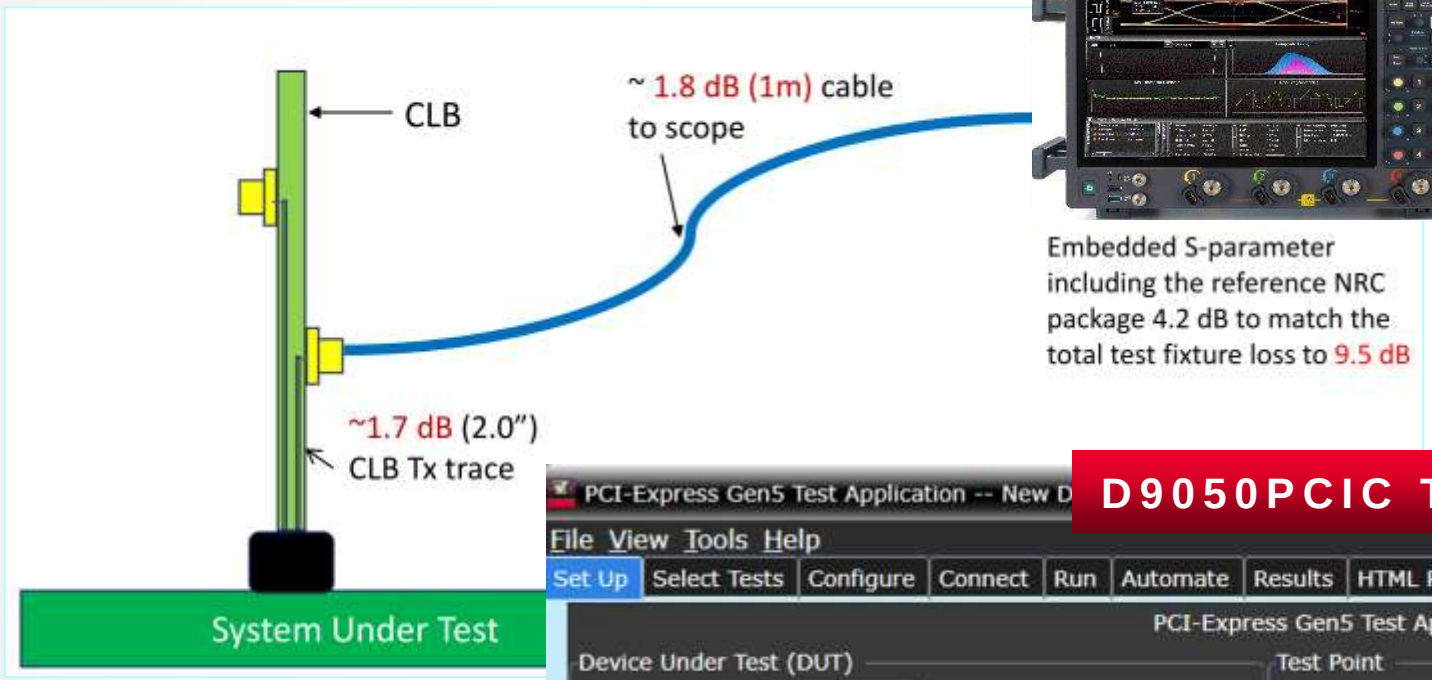
90000A (13GHz BW)				
Sample Rate	Clock Cycles	Max Jitter (ps)	Min Jitter (ps)	Pass/Fail
40 Gsa	160000	0.081500841	0.015917855	Pass

MXR (6GHz BW)				
Sample Rate	Clock Cycles	Max Jitter (ps)	Min Jitter (ps)	Pass/Fail
16GSa	160000	0.105338642	0.020580194	Pass

PCIe 5.0 32 GT/s CEM Tx Testing

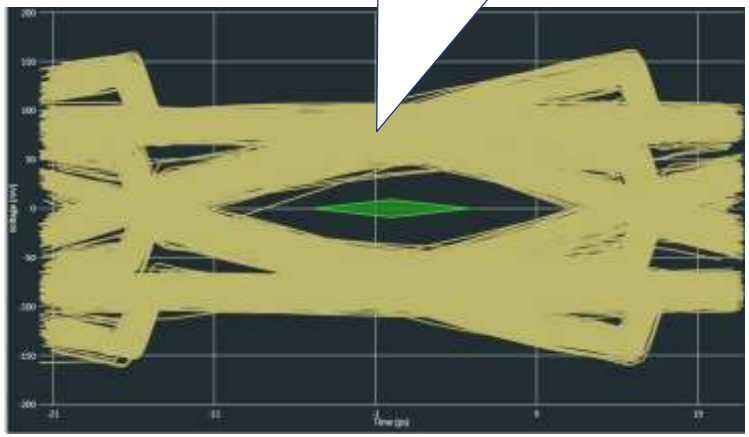
EX:SYSTEM BOARD; SSC ENABLE OR DISABLE

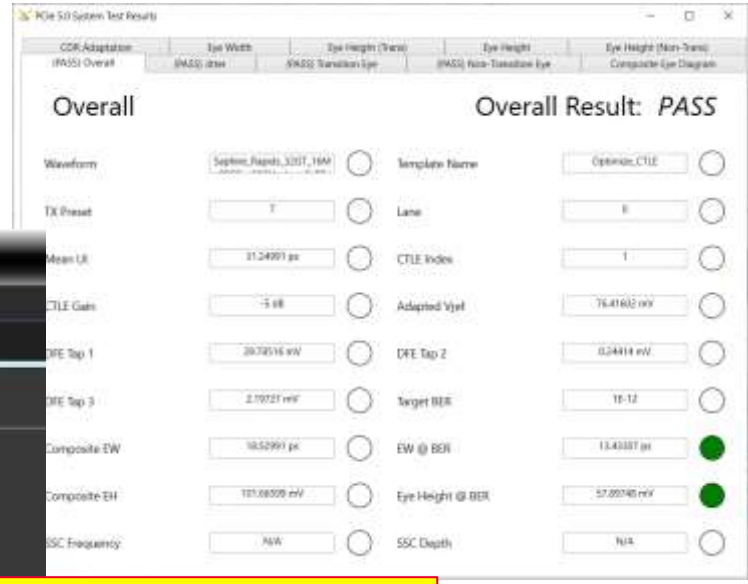
Keysight UXR-Series Real-Time Oscilloscope



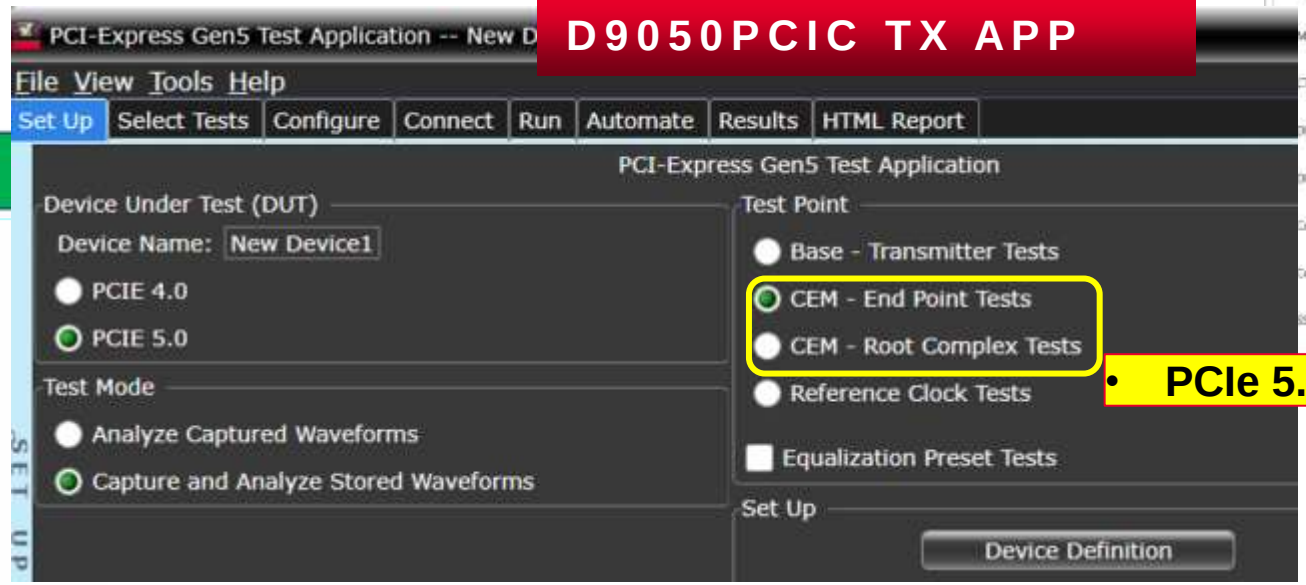
Embedded S-parameter including the reference NRC package 4.2 dB to match the total test fixture loss to 9.5 dB

Sigtest Phoenix





D9050PCIC TX APP



- **PCIe 5.0 CEM Spec. Tests**

Agenda

- **PCIe 5.0 CEM Tx/Rx Test Consideration**
  - Gen5 CEM Fixture timeline
  - Phy Test Specification update
  - 100MHz System Clock jitter test update
- **PCIe 6.0 64GT/s Test Consideration Pathfinding**
  - PAM4, SSC, SNDR, Top EH/EW
- **M8040A BERT solution for PCIe 5.0/6.0 LinkEQ Testing**
  - HS digital applications coverage
  - Redriver and EQ for long channel system board
  - Firmware evolution & HW performance
  - Fast, Accurate Rx Compliance SW
- **Summary**

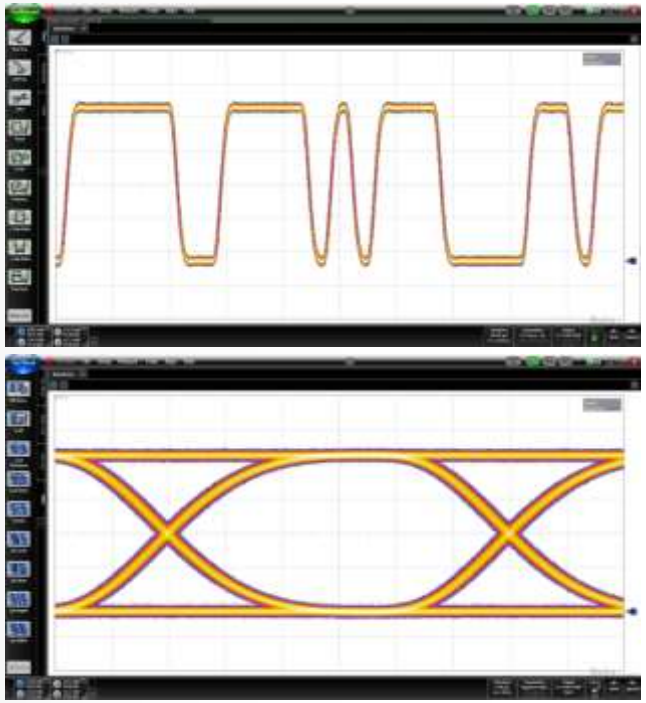
PCIe 6.0 Goals

KEY METRICS FOR PCIE 6.0

PCIe 6.0 Category	Objective
Data Rate	64 GT/s, 32Gbd, PAM4 (2x Gen5)
Latency	<10ns adder for Tx + Rx Over 32GT/s (include FEC Native BER 1e-6)
Key Applications	800G Ethernet, AI, Co-Processors, Accelerators
Reliability	As good as Gen5
Channel reach	-32dB at 16GHz (less to Gen5 Channel)
Power Efficiency	Better than Gen5
Low Power	Keeps L1 sub state, Addition of a new power state L0p
Plug n Play	Backward compatibility w/ Gen1-5 (Form Factors for CEM, M.2, Other?)
Other wants for Gen6	Not cost prohibitive to implement (HVM). Testable. Simple

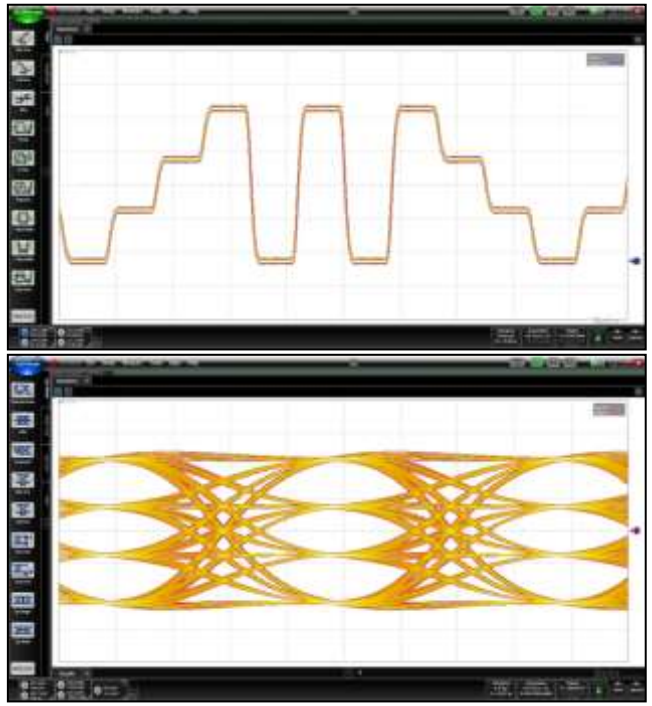
NRZ (Non-Return-to-Zero) vs. PAM (Pulse Amplitude Modulation)

NRZ (PAM2)



- 2 amplitude levels
- 1 bit of information in every symbol
  - ✓ 32 GBd NRZ = 32 Gb/s
  - ✓ PCIe 1,2,3,4,5 = NRZ

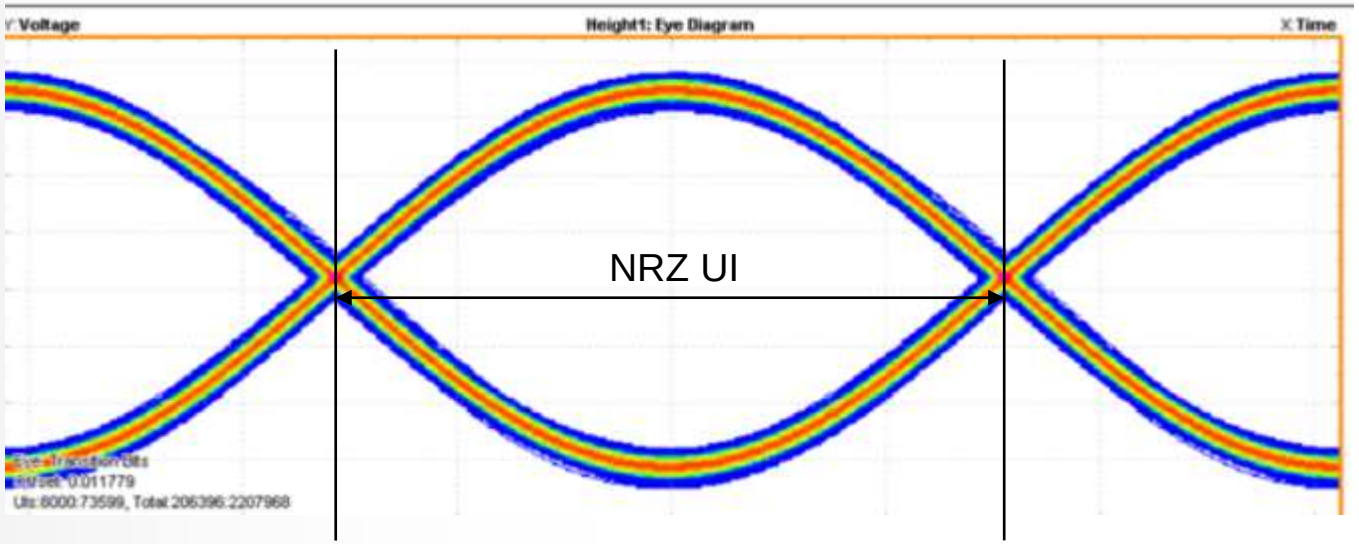
PAM4



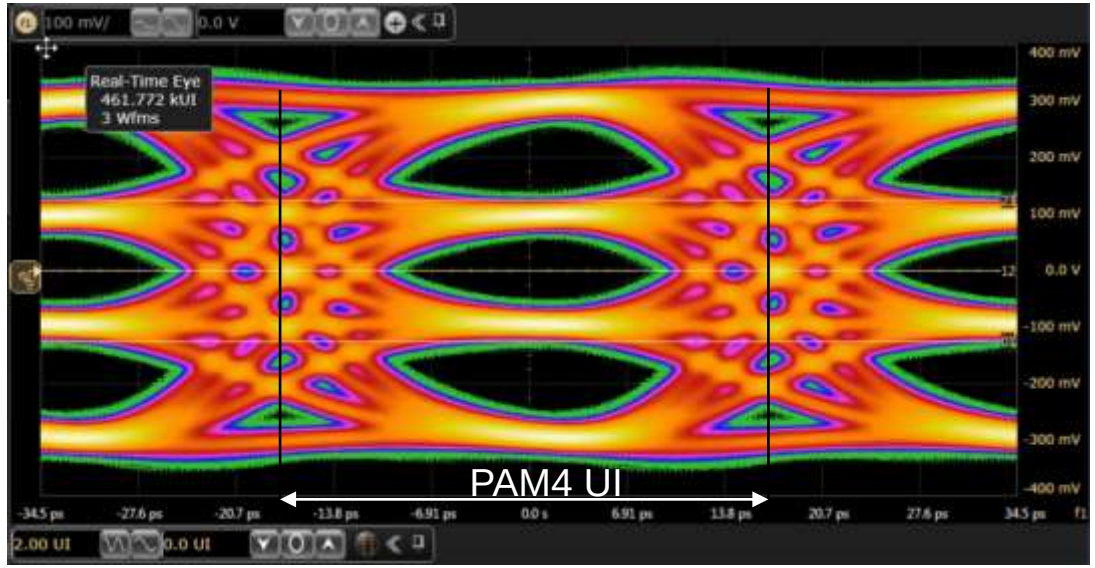
- 4 amplitude levels
- 2 bits of information in every symbol
  - ✓ ~ 2x throughput for the same Baud rate (FEC required)
  - ✓ 32 Gbaud PAM4 = 64 Gb/s
- Lower SNR, more susceptible to noise, loss, and reflections
- More complex TX/RX design, higher cost
- Nyquist frequency = 0.5*baud rate
  - PCIe 5.0 Nyquist Frequency = PCIe 6.0 Nyquist

PAM4 Signaling Challenges

- 1/3 reduction in amplitude (9 dB SNR degradation)
- ~ 33% UI timing loss due to level transitions



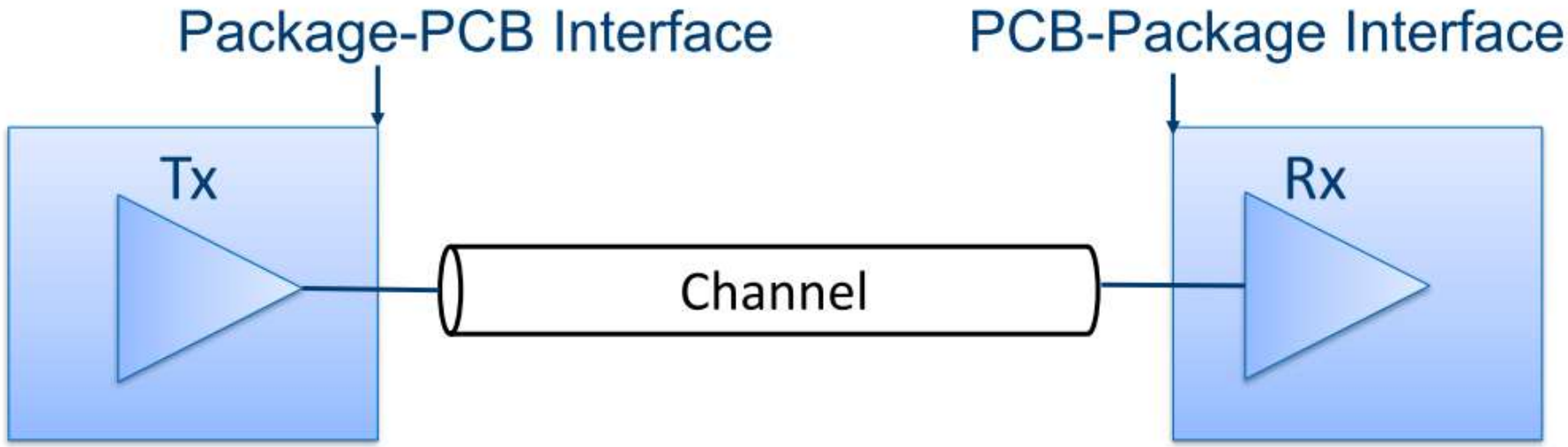
NRZ: Tx Clock Eye



PAM4 Tx Eye

Sensitivity to noise (xtalk, reflection, and other noise sources) is a key challenge
> 1.5x jitter reduction is necessary

PCIe 6.0 Channel Compliance



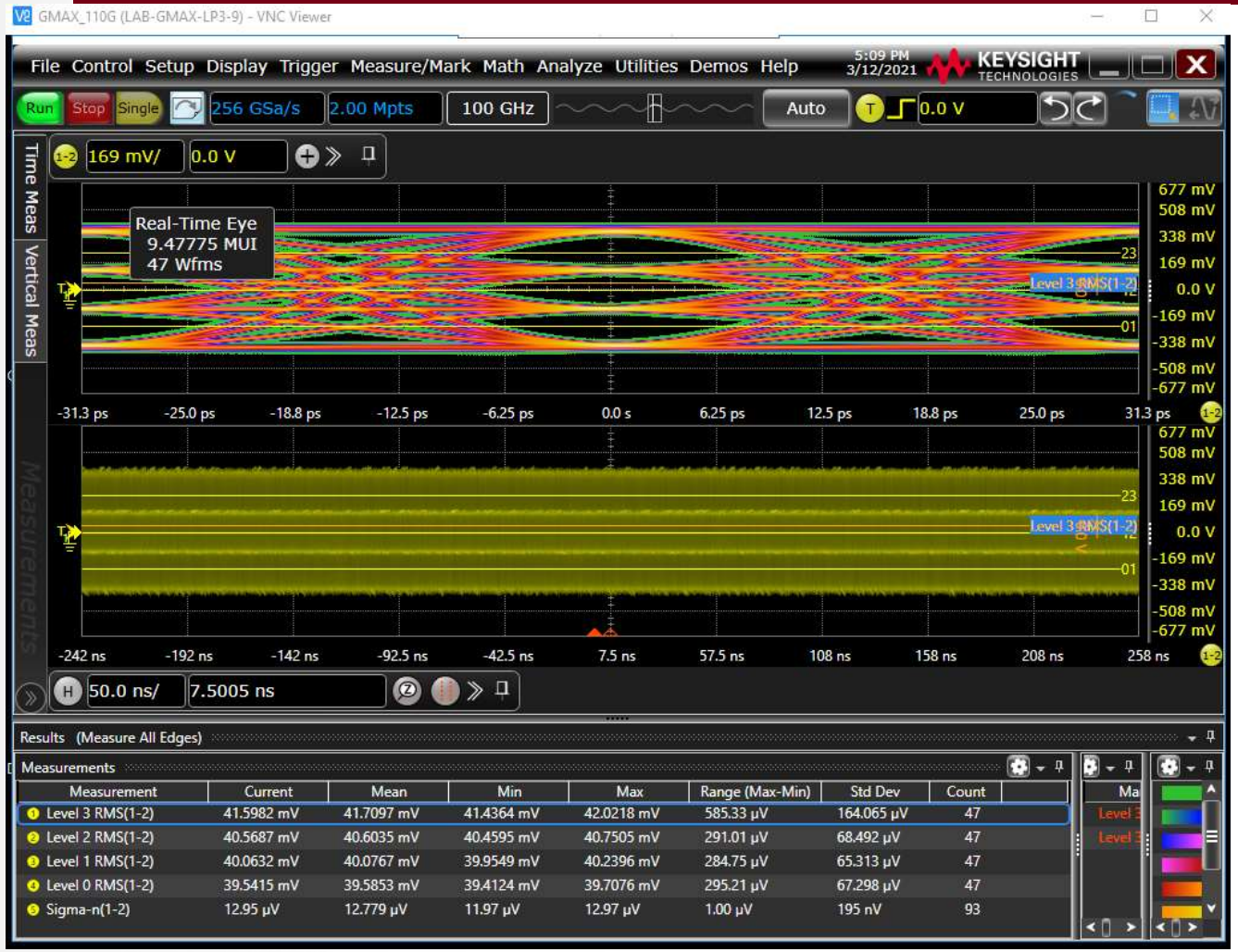
- Spec Package
- 4 tap TXLE (2 pre-cursors, 1 post-cursor)
- Spec Tx jitter only

- Spec Package
- Spec CTLE
- Spec DFE

Rev 0.7 Spec: Top EH >= 6.0 mV and Top EW >= 0.10 UI (3.125 ps) at BER = 1e-06 for a channel to be spec-compliant at 64 GT/s PAM4

PCIe 6.0 PAM4 Signal Challenge

PAM4 BRINGS NEW MEASUREMENT SOLUTION OPPORTUNITIES



64GT/s! (=32GBaud PAM4)
PCB Loss target of 1dB/inch
Eye Height=6 +/-0.5 mV(Top Eye)
Eye Width= 3.125 +/- 0.3ps (Top Eye)

- SNDR: Signal to Noise & Distortion Ratio >34dB
- R_{LM}: Ratio of Level Mismatch >0.95
- 12/48 Edge Jitter (similar to J4U)
- 100fs Ref Clock Jitter Limit (filtered)
- 4-tap TX Equalization
- New Reference Equalizer: CTLE+16 Tap DFE
- New FEC (low latency)
- Native BER of 1e-06
- Similar RX Test Method to PCIe 5

Transmitter SNDR from Base Spec.

PCI EXPRESS

PCI Express® Base Specification Revision 6.0 Version 0.71

PCI-SIG Draft Spec. 24 June 2021

8.3.3.12 Transmitter Signal-to Noise and Distortion Ratio ($SNDR_{TX}$) for 64.0 GT/s §

Signal-to-noise and distortion ratio (SNDR) is measured at the transmitter output using the Compliance Pattern (see § Section 4.2.14) with preset Q_0 (no Tx equalization), and the lanes not under test also transmitting the Compliance Pattern with preset Q_0. The recorded waveform must have a minimum of 250 repetitions of the compliance pattern. Measurements should be made with a 4th order Bessel-Thomson filter with a roll-off from DC value by 3 dB at 33 GHz to minimize the impact of scope high-frequency noise. The minimum scope bandwidth is 50 GHz.

A linear fit to the captured waveform and the linear fit pulse response, *p(k)*, and error vector, *e(k)*, are computed. The standard deviation of *e(k)* is denoted by σ_e. The linear fit pulse response *p(k)* and the error vector *e(k)* shall be computed with the pulse length of $Np = 600$ and pulse delay $Dp = 4$. For these computations, the number of samples per PAM4 symbol, M, must be equal to or greater than 32 and resampling can be used to meet this requirement. The standard deviation of *e(k)* is obtained from the measured PRBS portion of the compliance pattern.

$$SNDR = 10 \times \log_{10}\left(\frac{{p_{max}}^2}{{\sigma_e}^2 + {\sigma_n}^2}\right)$$

The parameter σ_n measures the uncorrelated RMS amplitude noise of each symbol level (including random noise and uncorrelated bounded noise effects), while not including ISI and jitter effects. Noise for each of the four PAM4 voltage levels, σ_L, is measured by using the PAM4 symbol 61 of the 64-UI long slow pattern for the corresponding voltage level that appears once in every repeat of the Compliance Pattern. For each voltage level L (where L = 0,1,2,3), the σ_L measurement is the result of eight independent measurements on eight evenly spaced sample points within the Unit Interval of symbol 61 in the run of 64 identical symbols. Each of the eight measurements denoted as $\sigma_{L,i}$ (where i=1..8) is calculated by using the following equations.

$$\sigma_n = \frac{1}{4}\left(\sigma_0 + \sigma_1 + \sigma_2 + \sigma_3\right)$$

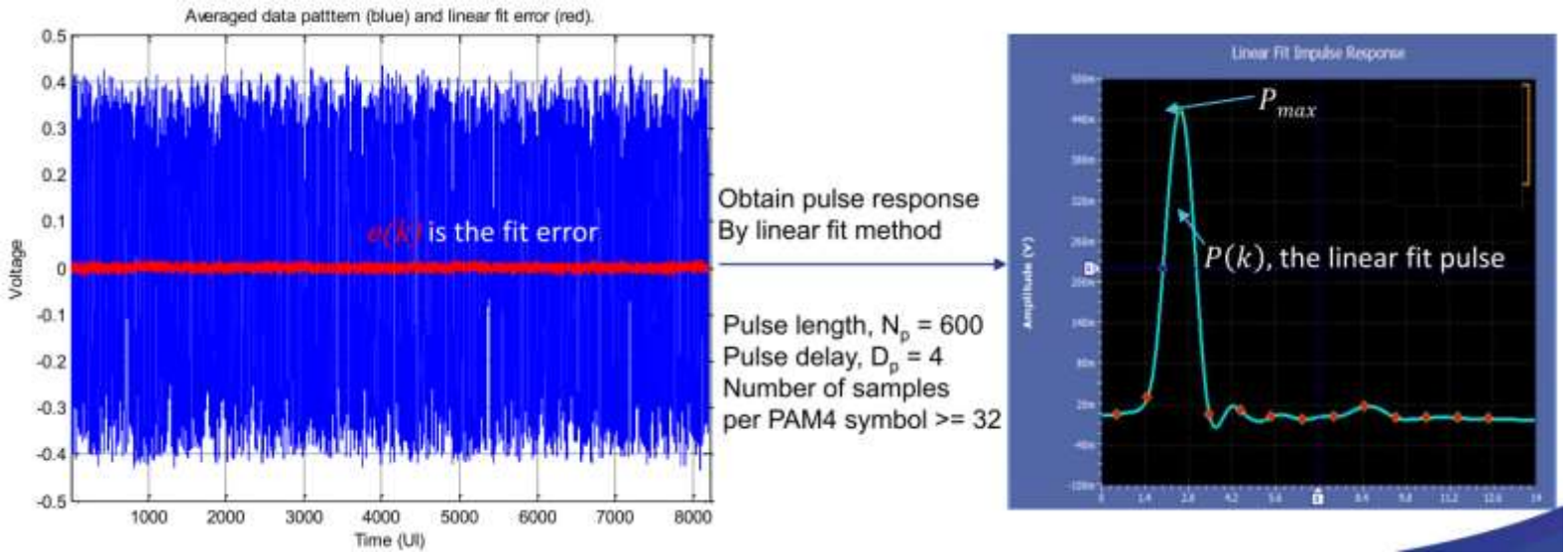
Tx SNDR Measurement Methodology

DOCUMENT FROM PCISIG

- Tx transmits 64GT/s compliance pattern that contains a section of PRBS23 pattern & four 64-UI long patterns – one for each PAM4 Voltage level
- The recorded waveform must have > 250 repetitions of compliance pattern
- A pulse response is constructed from the averaged waveform by linear fit method
- One repeat of the linear-model waveform is constructed by using the pulse response and superposition
- The difference between the measured *average waveform* & the linear model waveform is the error waveform e(k)

- σ_e is the standard deviation of the fit error *e(k)*
- σ_n is the average noise of the four PAM4 voltage levels
- $\sigma_n = \frac{1}{4}(\sigma_0 + \sigma_1 + \sigma_2 + \sigma_3)$

$$SNDR = 10 \times \log_{10}\left(\frac{{p_{max}}^2}{{\sigma_e}^2 + {\sigma_n}^2}\right)$$



Tx SNDR Measurement Methodology

- The parameter σ_n measures the uncorrelated RMS amplitude noise of each symbol level while not including ISI and jitter effects
- Noise for each of the four PAM4 voltage levels, σ_L, is measured by performing eight independent measurements on eight evenly spaced sample points within the Unit Interval of symbol 61 in the run of 64 identical symbols

Mean voltage, $\mu_{L,i} = \frac{1}{N_k} \sum_{k=1}^{N_k} V_{L,i,k}$, $L = 0, 1, 2, 3$ and $i = 1 - 8$

N_k = number of repetitions of the compliance pattern in the recorded waveform
N_k must be greater than 250.
$V_{L,i,p}$: voltage sampled at the i^{th} location within the UI of 61st symbol in the 64-UI long pattern of the PAM4 voltage level L in the k^{th} instance of the compliance pattern in the recorded waveform

Noise Variance, $\sigma_{L,i}^2 = \frac{1}{N_k} \sum_{k=1}^{N_k} \left(V_{L,i,k} - \mu_{L,i}\right)^2$

$\sigma_L = \sqrt{\frac{1}{8} \sum_{i=1}^{8} \sigma_{L,i}^2}$, $L = 0, 1, 2, 3$

$\sigma_n = \frac{1}{4}(\sigma_0 + \sigma_1 + \sigma_2 + \sigma_3)$

32Gbd x 8 samples = 256G Sa/s
Keysight UXR scope

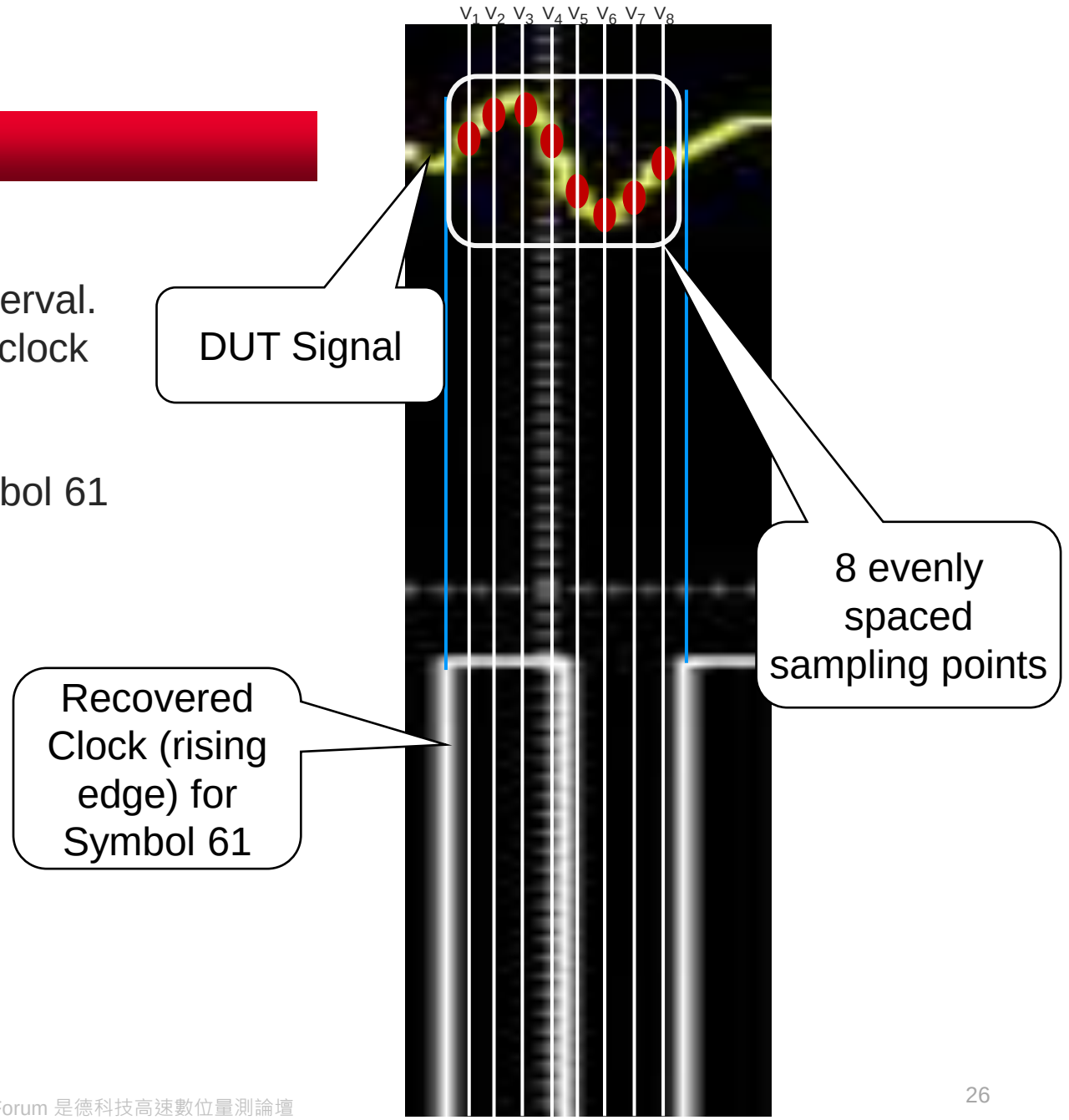
$$SNDR = 10 \times \log_{10}\left(\frac{{p_{max}}^2}{{\sigma_e}^2 + {\sigma_n}^2}\right)$$

Sigma N Calculation

SELECTING SIGMA N SAMPLE POINT

Clocks are always defined at the center of the unit interval. This corresponds to the rising edge of the recovered clock on real-time oscilloscopes.

For PCIe 6.0, 8 evenly spaced sample points for symbol 61 are used to calculate Sigma-n



PCIE 6.0 PAM4 Compliance Pattern

137 BLOCKS / 8768 SYMBOL

4.2.14 Compliance Pattern in 1b/1b Encoding §

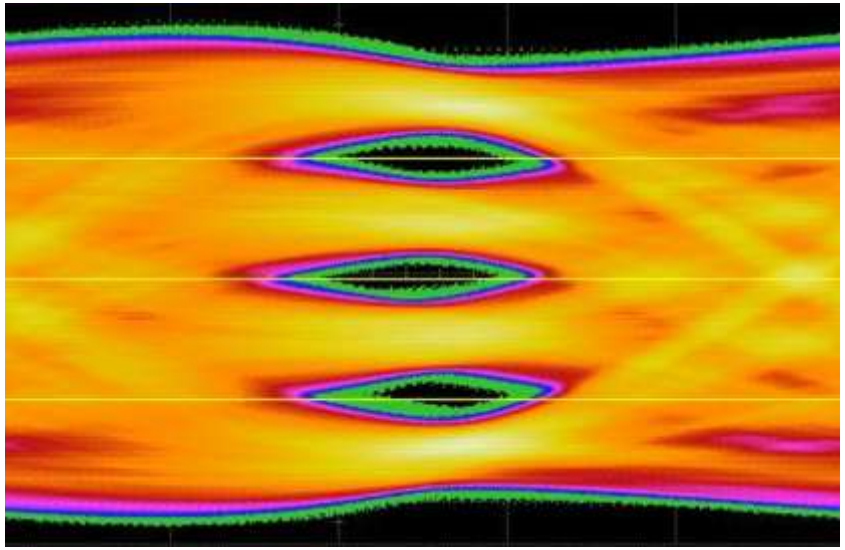
The compliance pattern consists of the following repeating sequence of 137 Blocks

1. One block, unscrambled: 64 UIs of 11b each (voltage level 3 throughout)
2. One block, unscrambled: 64 UIs of 00b each (voltage level 0 throughout)
3. Two unscrambled blocks of Toggle Pattern (Ch repeated 32 times for each block)
4. Two blocks with an unscrambled payload of the following: This is in hex format starting with the most significant Symbol. For example, in Lane 1, Block 5 (38_DA_CC_C4_E2_3F_1D_35_2B_35_63_CC_B2_CC_FF_FF), Symbol 0 is FFh and Symbol 15 is 38. Note that these are inserted for establishing DC balance.
   Lane 0, 8:
   Block 5: AA_AA_AA_AA_AA_AA_AA_AA_AA_AA_AA_AA_AA_AA_AA_AA
   Block 5: FF_FF_FF_FF_FF_FF_FF_FF_FF_FF_FF_FF_FF_FF_FF_FF (new)
   Block 6: 5A_37_88_75_83_2E_85_2A_AA_AA_AA_AA_AA_AA_AA_AA Block 6:
   5F_26_CC_65_C2_3B_C5_3F_FF_FF_FF_FF_FF_FF_FF_FF (new)
5. One block of EIEOS (unscrambled) – this resets the scrambler
6. 64 Blocks, each comprising of 16 Symbols of 00h scrambled. Please refer to Blocks 0 through 63 for the exact values in the corresponding Lane number in § Appendix K. .
7. One block, unscrambled: 64 UIs of 10b each (voltage level 2 throughout)
8. One block, unscrambled: 64 UIs of 01b each (voltage level 1 throughout)
9. 64 Blocks, each comprising of 16 Symbols of 00h scrambled. Please refer to Blocks 64 through 127 for the exact values in the corresponding Lane number in § Appendix K. .

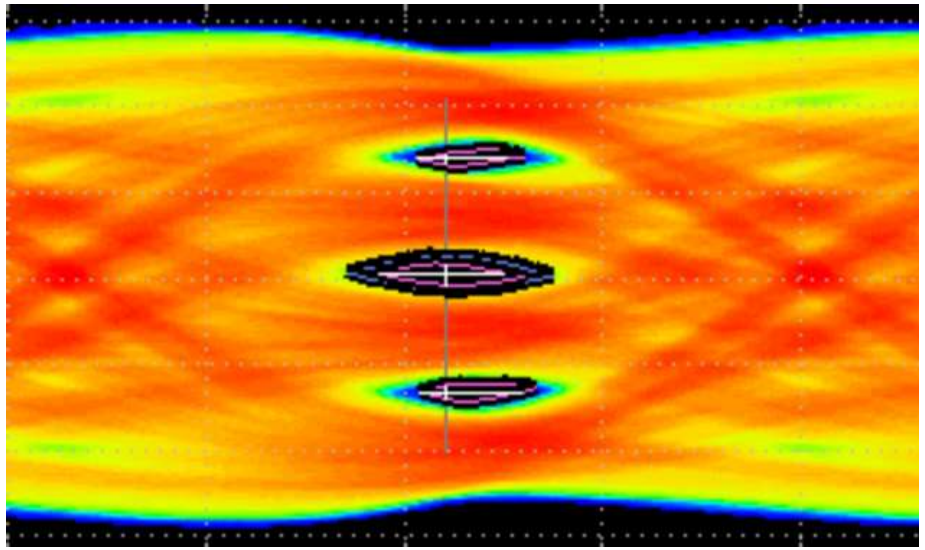
Block Type	Block content	Block Qty	Note
1	64 Symbol (11b)	1	Level 3
2	64 Symbol (00b)	1	Level 0
3	32 ”1100b”	2	Toggle Pattern
4	16 Symbol Unscrambled Payload	2	(Lane# depends)
5	EIEOS	1	
6	16 Symbol (00h) Scrambled	64	(Lane# depends)
7	64 Symbol (10b)	1	Level 2
8	64 Symbol (01b)	1	Level 1
9	16 Symbol (00h) Scrambled	64	(Lane# depends)

PAM4 Eye Comparison (53Gbd on 70GHz scopes)

10 BITS UXR VS OTHER 8 BITS SCOPE



UXR (10 bits)



8 bits RT Scope

Measurement	UXR (40 GHz 4BT)	8 bits Scope (40 GHz 4BT)
Eye Width 1 (ps)	3.0	2.5
Eye Width 2 (ps)	3.5	3.2
Eye Width 3 (ps)	3.4	2.2
Eye Height 1 (mV)	22.6	13.9
Eye Height 2 (mV)	30.7	23.4
Eye Height 3 (mV)	28.6	13.9

Average Eye Width 25% Better

Average Eye Height 60% Better

Agenda

- **PCIe 5.0 CEM Tx/Rx Test Consideration**
  - Gen5 CEM Fixture timeline
  - Phy Test Specification update
  - 100MHz System Clock jitter test update
- **PCIe 6.0 64GT/s Test Consideration Pathfinding**
  - PAM4, SSC, SNDR, Top EH/EW
- **M8040A BERT solution for PCIe 5.0/6.0 LinkEQ Testing**
  - HS digital applications coverage
  - Redriver and EQ for long channel system board
  - Firmware evolution & HW performance
  - Fast, Accurate Rx Compliance SW
- **Summary**

M8040A High speed digital solution coverage

PCIE 6.0 HW READY RX BERT SOLUTION

PCI Express 6.0 5.0 4.0
64G/ 32G/16G/8G/5G/2.5G

mipi alliance
MIPI M-Phy Gear4

USB3.2/ USB4 /TBT4

CEI-03.1
- CEI-28G-SR/-MR
- CEI-25G-LR

Serial Attached SCSI
SAS-4/SAS-3
22.5G/12G

CCIX
25G/20G

SERIAL ATA
SATA Gen3
6G/3G

IEEE 802.3
- 200GAUI-4 PAM4 C2C
- 400GAUI-8 PAM4 C2C

CEI-04.0
- CEI-56G-MR/-LR PAM4

OIF

Consumer/Computer:
TBT 3.0 20G

Electrical TRX:
- CEI-04.0
  - CEI-56G-VSR PAM4
- CEI-03.1
  - CEI-28G-VSR[3)]
- IEEE 802.3
  - 200GAUI-4 PAM4 C2M
  - 400GAUI-8 PAM4 C2M

Optical TRX:
- IEEE 802.3
  - 25GBASE-LR/-ER/-SR
  - 100GBASE-LR4/-ER4/-SR4
  - 200GBASE-FR4/-LR4/-DR4
  - 400GBASE-FR8/-LR8
  - 400GBASE-DR4
- MSA
  - 100G-CLR4 MSA
  - 100G CWDM4 MSA
  - 100G 4WDM-10/-20/-40 MSA
  - 400G-FR4 100G lambda MSA

M8040A/M8046A ED EQ + M8047A

M8047A: dual stage CTLE + linear amplifier

+

M8046A: 16 tap EQ

- The M8047A + M8046A offers an adjustable dual stage CTLE + 16 tap FFE which enables the M8040A to deal with any PCIe 4.0 compliant backchannel for RX testing and LinkEQ TX testing including response time testing.
- First test with a real PCIe 5.0 32G root complex have shown that the M8047A can be used at 32G.
- The M8047A control is fully integrated into the M8070B GUI and will be integrated into the N5991 PCIe test automation soon.
- The M8047A list price is just 5k USD

For symbol rates up to 32 Gbaud:

- Up to 13 dB at 32.4 Gbaud NRZ.
- Up to 5.5 dB at 29 Gbaud PAM4.
- Up to 5.1 dB at 26.5625 Gbaud PAM4
- FFE with 55 presets for PAM4 and 120 presets for NRZ. See figure below.
- No Equalizer license is needed below 32 Gbaud.

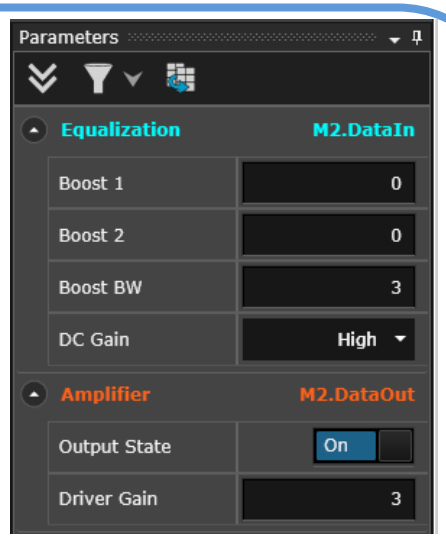
M8046A EQ

For symbol rates above 32 Gbaud:

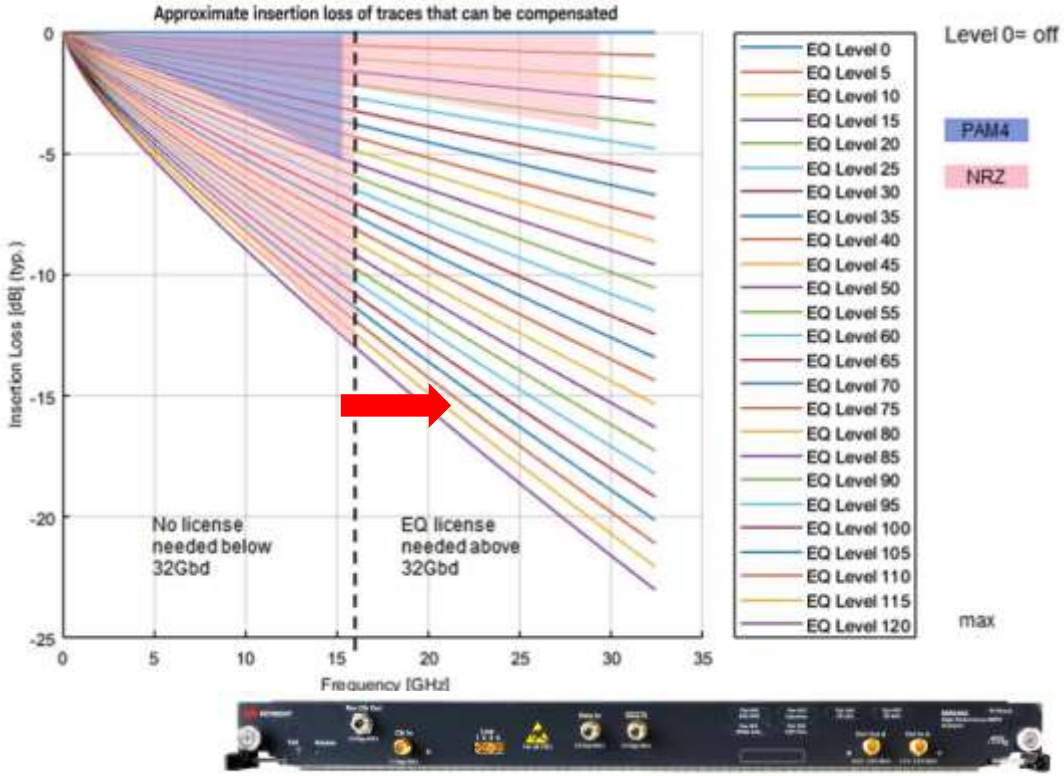
- Up to 3 dB at 58 Gb/s for NRZ signals. (requires M8046A-0A3 and -A64): 120 presets for NRZ, FFE.

\+

M8047A



Parameter	
Output	On / Off
Output driver gain settings	0 to 3
EQ Boost 1	0 to 7
EQ Boost 2	0 to 7
EQ Boost bandwidth	0 to 3
EQ DC gain	Low / High



Max. IL ISI channel the M8047A+M8046A can Achieve

MAX IL FOR ERROR FREE@ 32GBPS(16GHZ)

- **Understanding the Max. IL limitation of M8047A+M8046A for Gen5**

Preset 5, 800mV
Modified
Compliance
pattern

M8041A-801
SMP short cable

Pair#28 (13.18”)

M8041A-801
SMP short cable

Max. IL ISI channel the M8047A+M8046A can Achieve

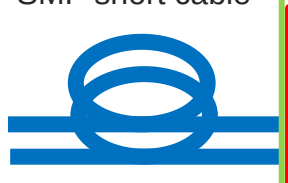
MAX IL FOR ERROR FREE@ 32GBPS(16GHZ)

Preset 5, 800mV Modified Compliance pattern

M8041A-801
SMP short cable

Pair#28 (13.18”)

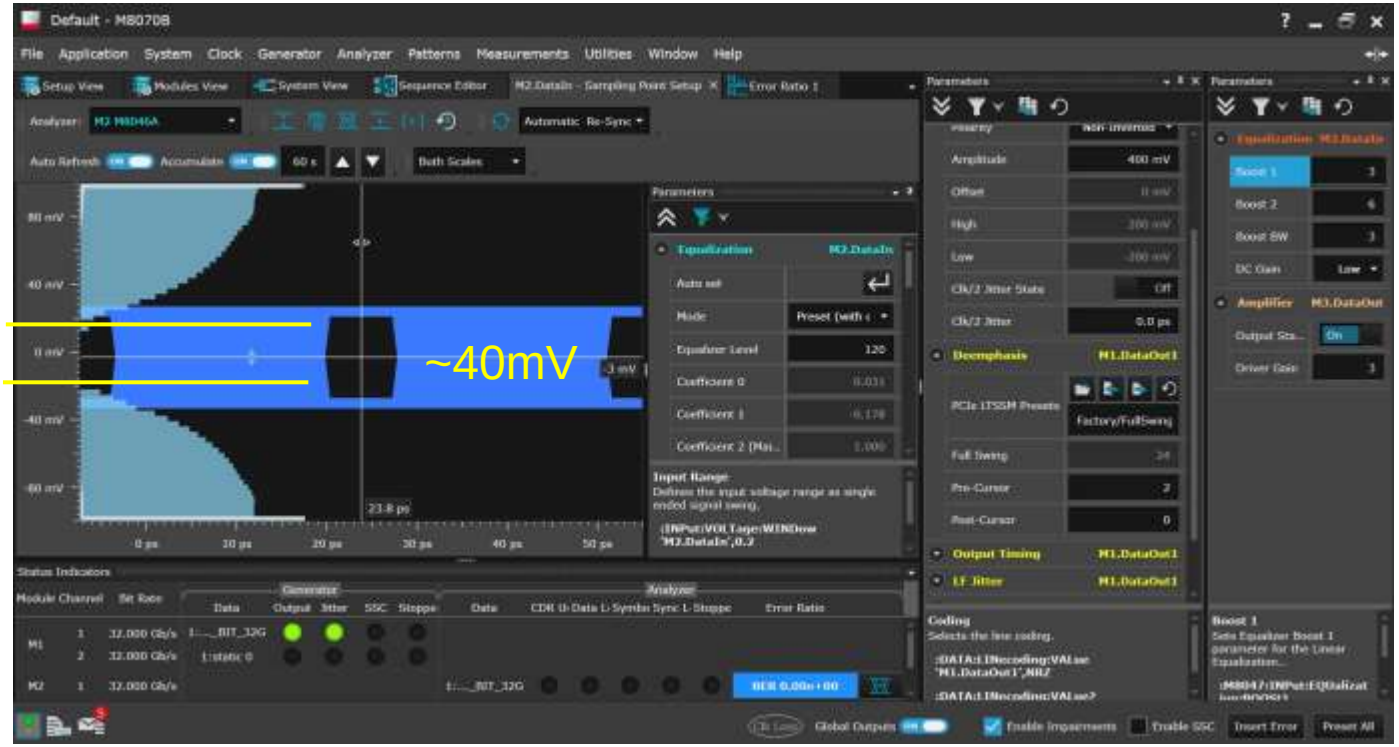
M8041A-801
SMP short cable



Boost1=3
Boost2=6
Boost.BW=3
DC Gain=Low
Driver Gain=3

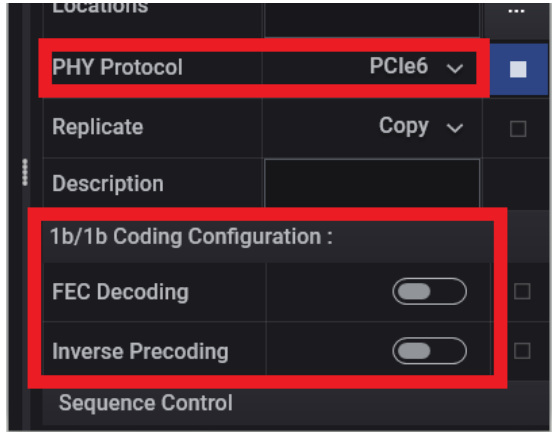
-33.4dB

- **IL=-33.4dB, before M8047A, and M8046A EQ**
- **Eye open~40mV**



M8040A FW evolution with Specification change

32GT/S RXEQ TEST WITH SSC "ENABLE OR DISABLE"



M8070B FW Ver.8.0 New Features for PCIe:

1. **SKPOS filtering** now up to PCIe 6, 64 GT/s
2. Added **speed bypass mo**de for "L0 (local oscillator) /Recovery" training
3. Added LTSSM for other than lane 0 – configuration
4. Reference clock multiplier (PG PLL) support with SSC (spread spectrum clocking) transfer from 100 MHz ref clock to 64 Gbaud

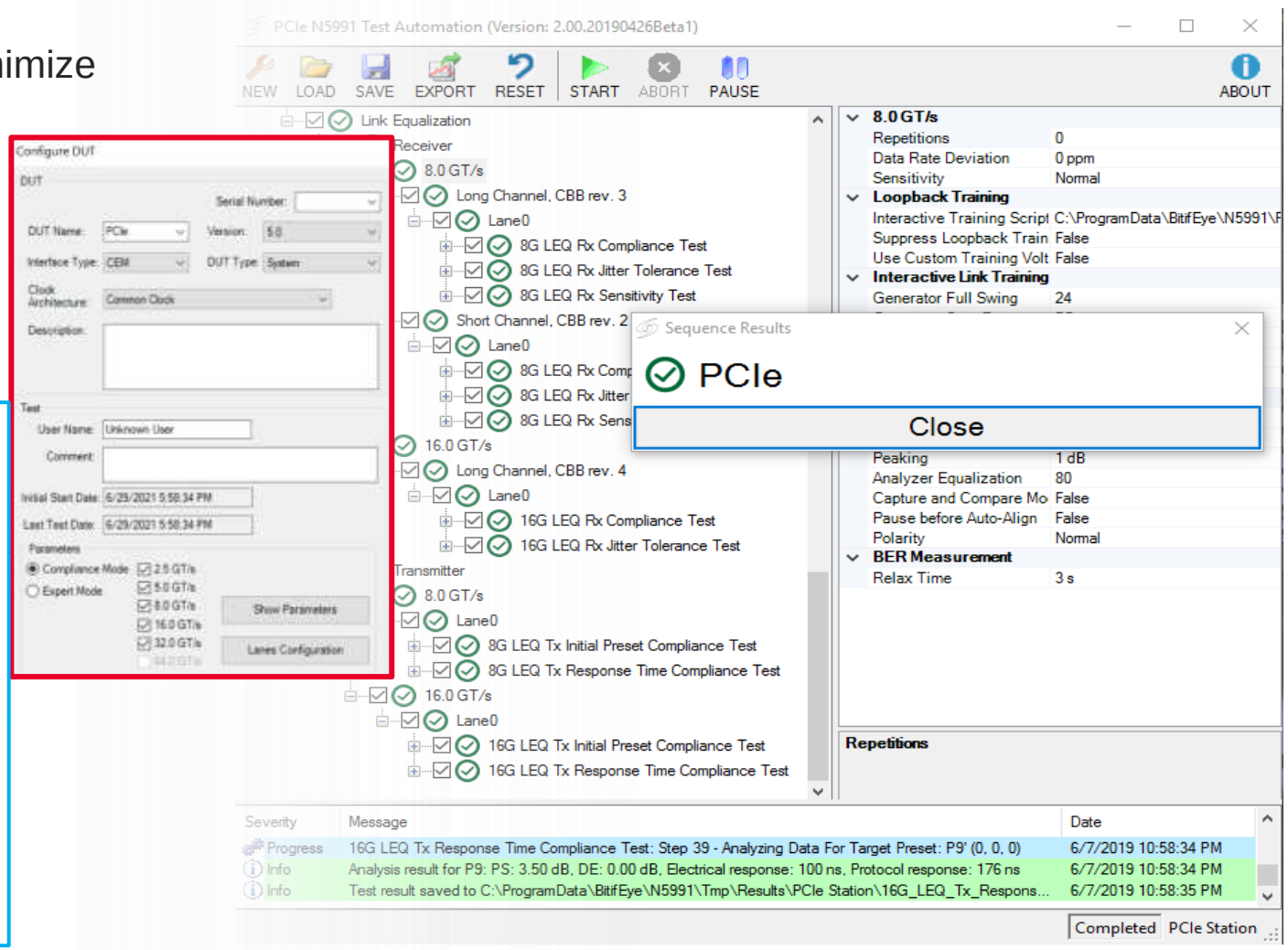
M8046A CDR performance:

Selectable loop type	First and second order PLL - see figure below for description	Yes
Tunable loop bandwidth [3]		2 to 20 MHz. For second order PLL the range depends on selected peaking. 4 to 16 MHz with PAM4 and symbol rate > 32.4 Gbaud [1]
Loop bandwidth accuracy		± 30% typical for symbol rates ≥ 4.9 Gbaud
Transition density		25-100%
Clock recovery peaking range		Up to 4 selectable settings (dependent on loop bandwidth and b
Acquisition	Input symbol rate must be within the range of ± 500 ppm of the set symbol rate	± 500 ppm typical
Tracking range	SSC can be tracked when symbol rate is set to center frequency. SSC frequency ≥ 30 kHz	± 3000 ppm typical (for symbol rate up to 32.4 Gbaud)

N5991PxxA – PCIe Test Automation

RX TEST AUTOMATION SOFTWARE

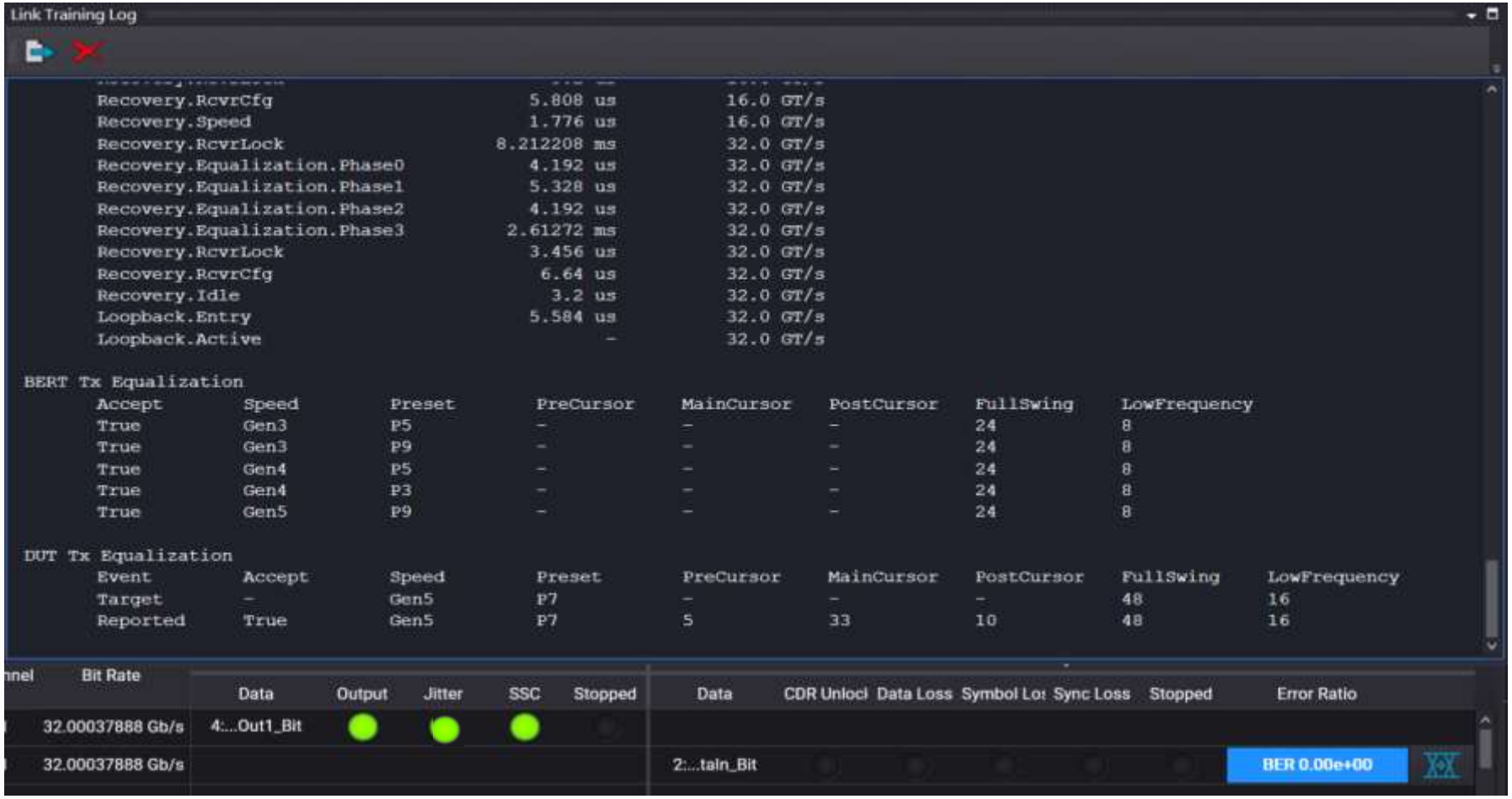
- Guided and automated stress signal calibration minimize user interaction and help to reduce errors
- Test beyond compliance
  - TxEQ matrix scan for 32 GT/s, 16 GT/s and 8 GT/s
  - JTOL test for 32 GT/s, 16 GT/s and 8 GT/s
  - Sensitivity Test for 8 GT/s



Gen5 System Platform loopback

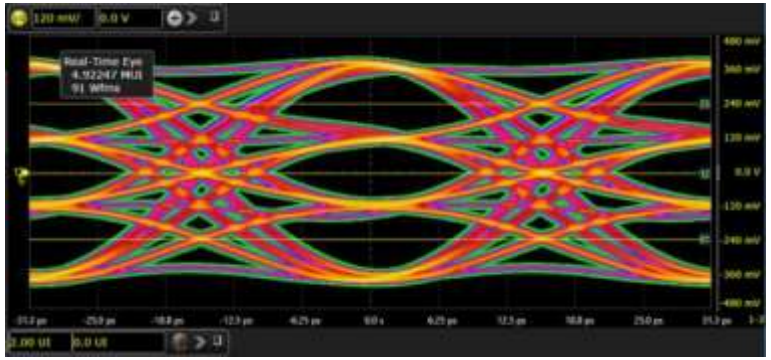
SSC ENABLE AND DISABLE

Result	SJ Frequency [MHz]	SJ Amplitude [ps]	Allowed Bit Error []	Measured Bit Error []	Final Generator Preset	Final Generator Pre-shoot [dB]	Final Generator De-emphasis [dB]
pass	100.00	3.125	1	0	P9	3.66	0.00



Summary

BEST SOLUTION FOR PCIE 5.0 TO 6.0

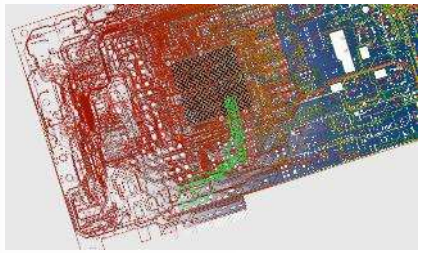


1. UXR is the best choice for PCIe 6.0 PAM4, Best Signal Integrity, Lowest noise/jitter, 10Bit ADC, 256GSa/s
2. M8040A HW ready for PCIe 6.0
3. M8040A provide widest High-Speed Digital Applications coverage
   - (PCIe 5.0/4.0/3.0/2.0/1.0, U.2, M.2, SATA3.0, SAS12G/24G, CCIX, USB4, Thunderbolt3/4, USB3.2, IEEE 802.3bs, 802.3cd, 802.3CK, CEI 56G/28G, 25G PON)
4. Keysight provide M8047A Re-driver for long channel system test
5. M8040A provide best CDR performance in market
6. New Four LTSSM Loopback paths – more flexible in testing and debug
7. Best, Most Accurate, Fastest Compliance software for calibration and testing in Gen5 market

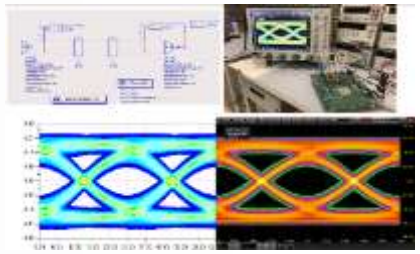
PCI Express® 5.0 & 6.0 – Keysight Total Solution

Physical Layer – System Simulation

ADS Design Software



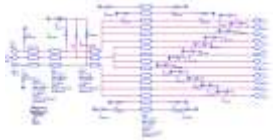
SIPro/PIPro



Simulation to Measurement Correlation

Complete System Simulation
From Pre-layout analysis to Post-layout extraction

Physical layer – interconnect design



ADS design software

86100D DCA-X/TDR

N5227B PNA w/ PLTS

Verify PCIe 5.0 Compliant Channels
Verify Return Loss Compliance
Capture break-out channel S-Params

Physical layer-transmitter test

UXR-Series, Z-Series Real-Time Oscilloscopes

D9050PCIC PCI Express 5.0 TX Electrical compliance software

86100CU-400 PLL and Jitter Spectrum Measurement SW

DSA UXR-Series & Z-Series Real-Time Oscilloscopes

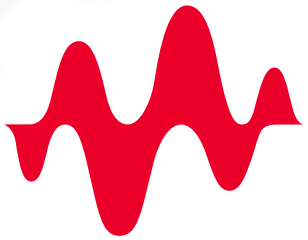
Physical layer-receiver test

M8046A J-BERT High Performance BERT w/ integrated CDR + M80454A Interference Source

M8049A-1 Substitute PCIe 5 BASE Channel board

N5991PB5A
PCIe 5.0 32GT/s RX Test software

Automated RX Test software
- Accurate, Efficient
- Comprehensive RX Testing



KEYSIGHT
TECHNOLOGIES

Thank You